

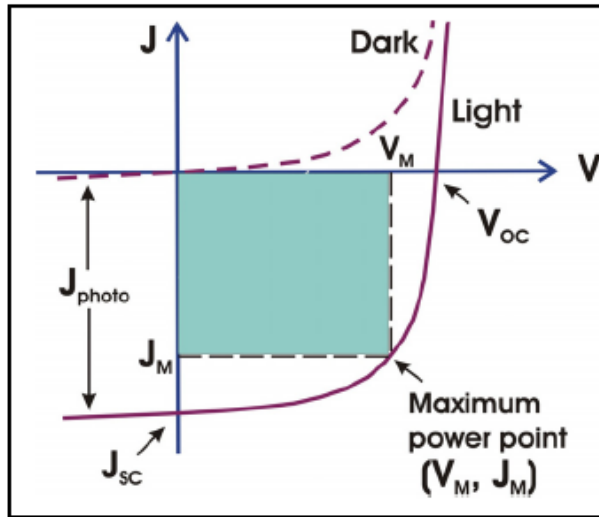
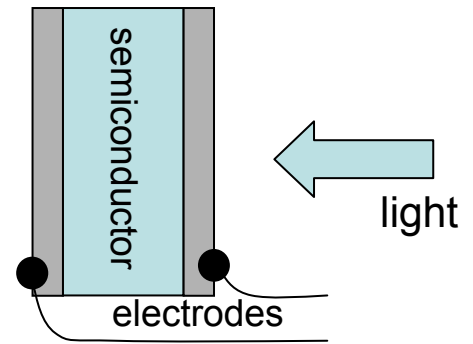
Materials, Electronics and Renewable Energy

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- Inorganic semiconductor solar cells

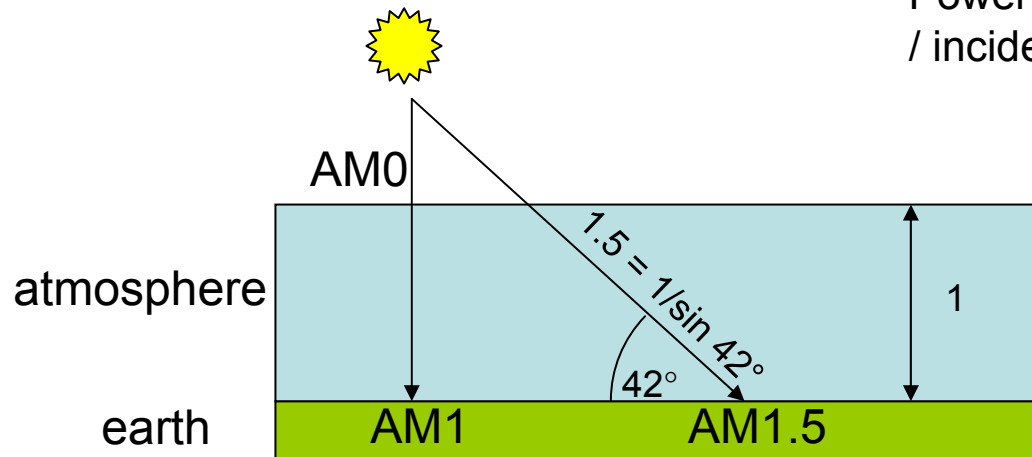
Current-Voltage characteristic for photovoltaic



Some definitions:

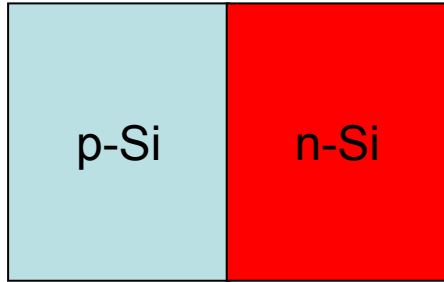
- V_{oc} , open-circuit voltage
- J_{sc} , short-circuit current density
- Fill Factor $FF = V_M J_M / V_{oc} J_{sc}$
- Max Power Out $P_m = V_M J_M = FF * V_{oc} J_{sc}$
- Quantum efficiency = $J_{sc} / (e \times \text{photon flux incident})$
- Power conversion efficiency = $P_m / \text{incident solar energy flux}$

Must specify solar spectrum:



AM = "air mass"

Silicon p-n junction



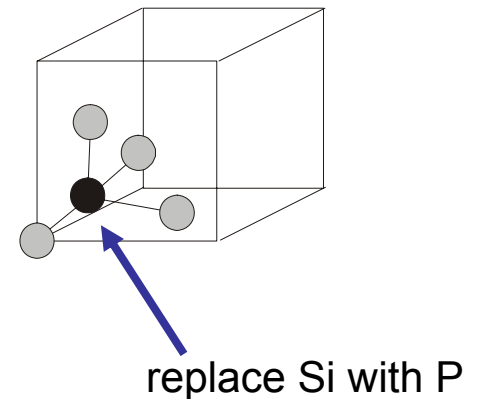
Doping

n-type

- Substitute Si with pentavalent impurity, e.g. P
- Extra electron donated to conduction band

p-type

- Substitute Si with trivalent impurity, e.g. B
- Electron removed from valence band
- \equiv adding a hole



Fermi level \equiv chemical potential

Sets electron and hole populations by Boltzmann statistics

$$n = N_c \exp((E_F - E_c)/kT)$$

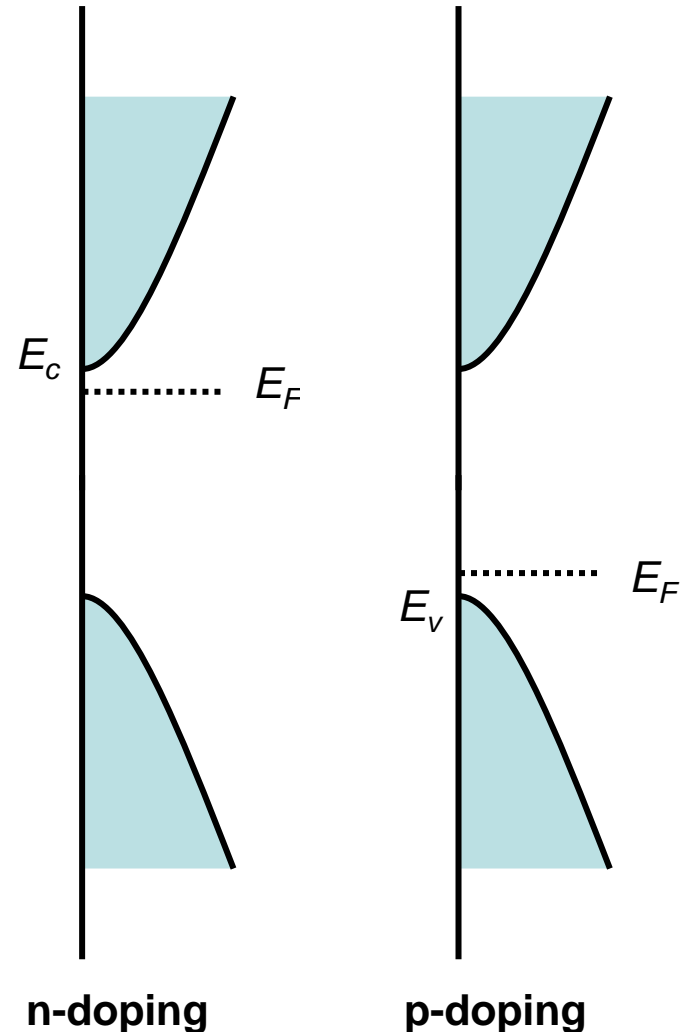
$$p = N_v \exp((E_v - E_F)/kT)$$

n-doping

- most dopants ionised at room temperature
- electron concentration = dopant concentration
- Fermi level close to conduction band

p-doping

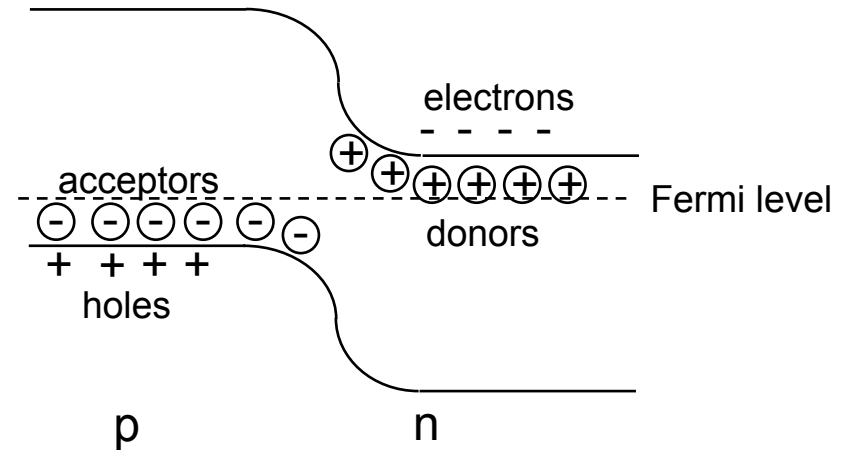
- hole concentration = dopant concentration
- Fermi level close to valence band



The p-n junction

Near the junction

- electrons from n-type fill up holes in p-type
- forms “depletion region”
- creates a dipole



Dark current

$$J = J_s \left(e^{\frac{eV}{nkT}} - 1 \right)$$

should be 1 (but isn't)

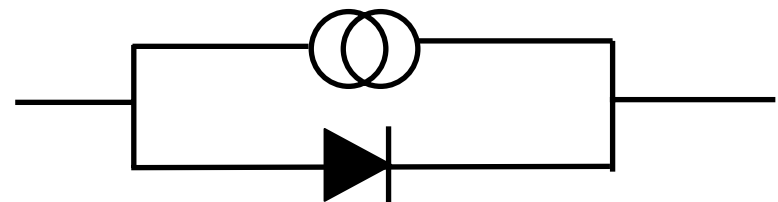
Approximate physics

- carriers must jump over barrier at depletion region
- barrier height depends on applied voltage

Under illumination

$$J = J_s \left(e^{\frac{eV}{nkT}} - 1 \right) - J_{ph}$$

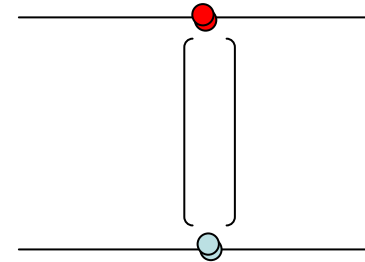
← photocurrent



What determines the photocurrent?

One photon absorbed

- Either
one electron and one hole get out
- Or
one electron and one hole recombine



Drift and diffusion

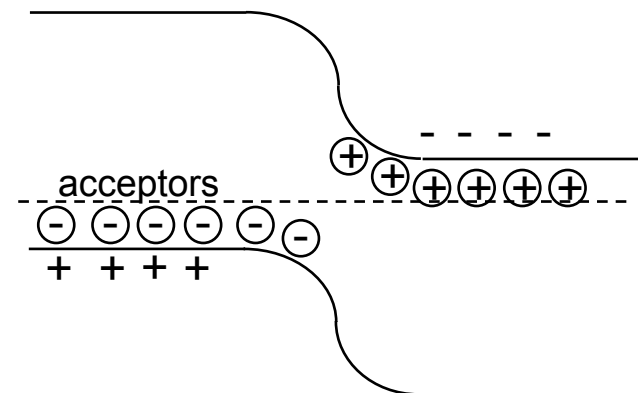
$$J_n = \underset{\substack{\text{mobility} \\ \downarrow \\ \text{drift}}}{eE\mu n} + \underset{\substack{\text{diffusion coefficient} \\ \downarrow \\ \text{diffusion}}}{eD \frac{dn}{dx}}$$

$$D = \frac{kT\mu}{e}$$

due to *random* thermal motion

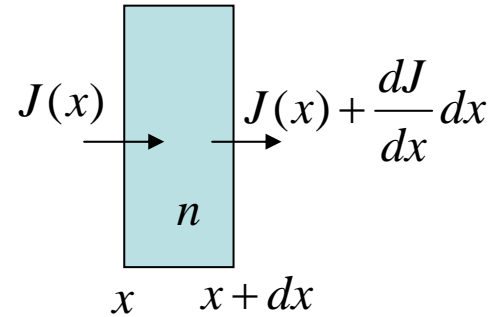
Si p-n junction

- Device is thick (to absorb light, $\sim 200 \mu\text{m}$)
- Depletion region is thin (~ 10 's of nm)
- No field in most of device
- Current extracted by diffusion

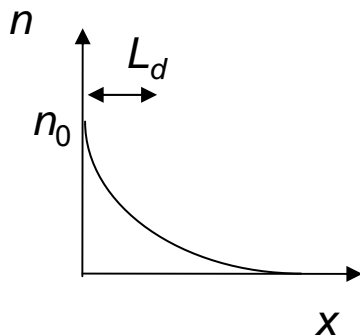


Diffusion and recombination

$$\begin{aligned}\frac{dn}{dt} &= \frac{1}{e} \frac{dJ}{dx} - \frac{n}{\tau} \quad \leftarrow \text{recombination lifetime} \\ &= D \frac{d^2 n}{dx^2} - \frac{n}{\tau} \\ &= 0 \quad \text{at steady state}\end{aligned}$$



Solution:



$$n = n_0 e^{-x/L_d}$$

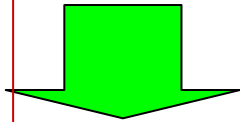
$$L_d = \sqrt{D\tau}$$

diffusion length

Carriers only diffuse a limited distance ($\sim \mu\text{m}$'s) before recombining

Practical Silicon Solar Cells:

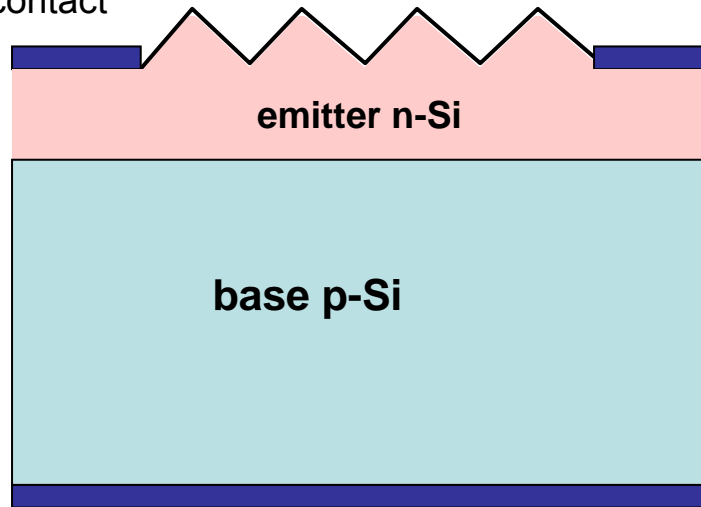
front contact –
'shading' reduces
light collection



incident light

textured surface with anti-reflection
coating (note: Si has reflection coefficient
of about 40% - AR coating with n about 2
is essential)

front contact



emitter n-Si

base p-Si

thin heavily-doped 'emitter' – ($0.3\ \mu\text{m}$)–
- conductivity needed for charge
collection, but high doping level
reduces diffusion lengths for holes

thick lightly-doped 'base' – ($300\ \mu\text{m}$)–
low doping level to give large diffusion
range for electrons. Thick enough to
absorb most of incident light

rear contact

efficiencies of about 20%
achieved since the late
1980's.

rear contact – will cause
'recombination' of minority carriers that
reach it

Recombination mechanisms include:

direct recombination (and can then emit photons)

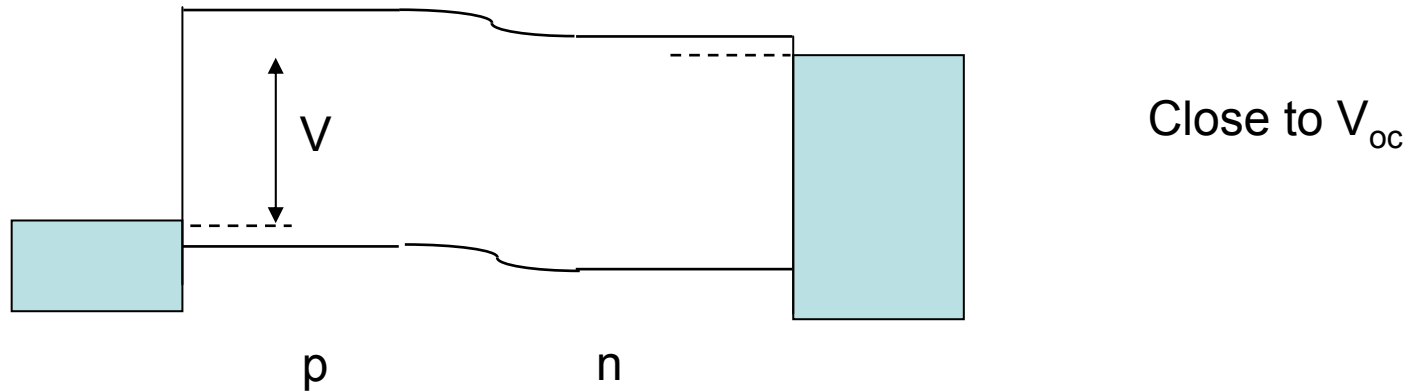
'recombination' at rear contact (if electrons diffuse this far) and front contact (holes)

Shockley-Read-Hall recombination. One of other charge gets trapped at a defect, and is eventually neutralised by capture of the other charge

Auger recombination – e.g. two electrons collide, one is de-excited (to a hole state in the valence band) and the other excited within the conduction band (and then cools rapidly to the bottom of the conduction band).

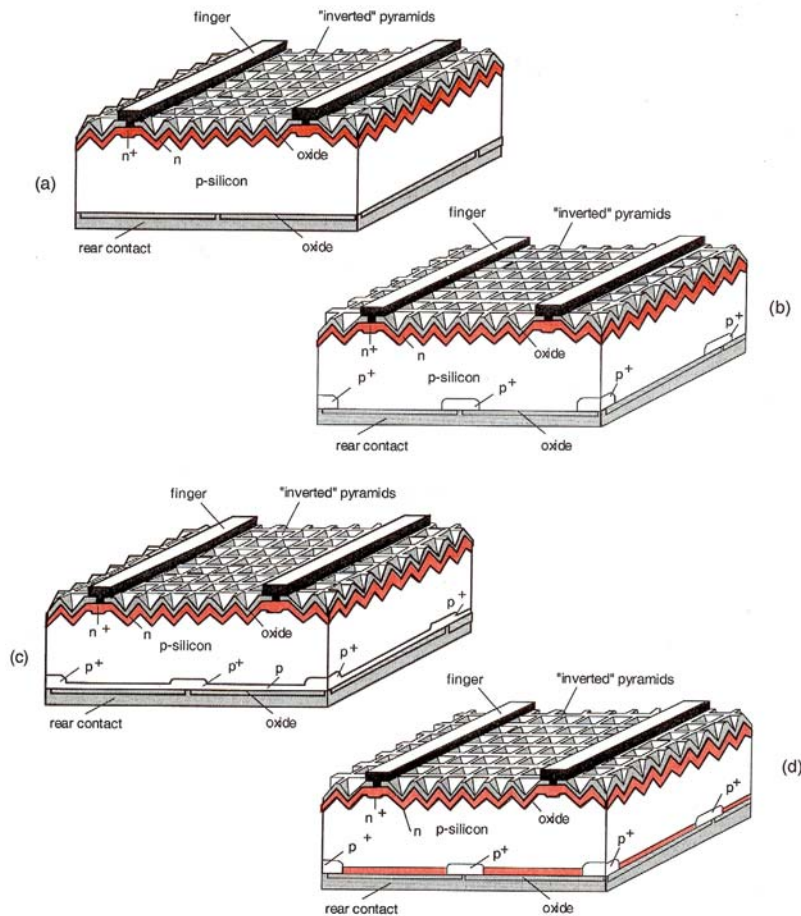
What about the voltage?

- Avoiding recombination is not enough
- Need to collect carriers at a potential close to the bandgap



- p and n doping helps to achieve “ohmic” contacts which avoid energy losses
- in general, metal-semiconductor interfaces are a mess

Practical Silicon Solar Cells: cont.



4 high efficiency Si solar cells: (a) passivated emitter and rear cell, (b) passivated emitter, rear locally diffused cell (up to 24% efficiency in early 1990s), (c) passivated emitter rear totally diffused cell, (d) passivated emitter, rear floating junction cell.

[After Green and Hansen (1998) UNSW, Australia]

Economic limits to crystalline silicon:
[current technology re-uses 'scrap' silicon from the microelectronics industry – costs may rise if demand for scrap silicon exceeds supply]

Large quantities of silicon are required (thick cells are needed to absorb light effectively)

- Cleanest silicon – microelectronics grade wafers sawn from single-crystal ingots
- Multicrystalline silicon ingots – solidify molten silicon into rectangular cross-section multicrystalline ingots. Polycrystalline, and still require sawing to correct thickness sheets.
- Draw from melt as 'sheet' or 'ribbon'

Virtues of crystalline silicon:

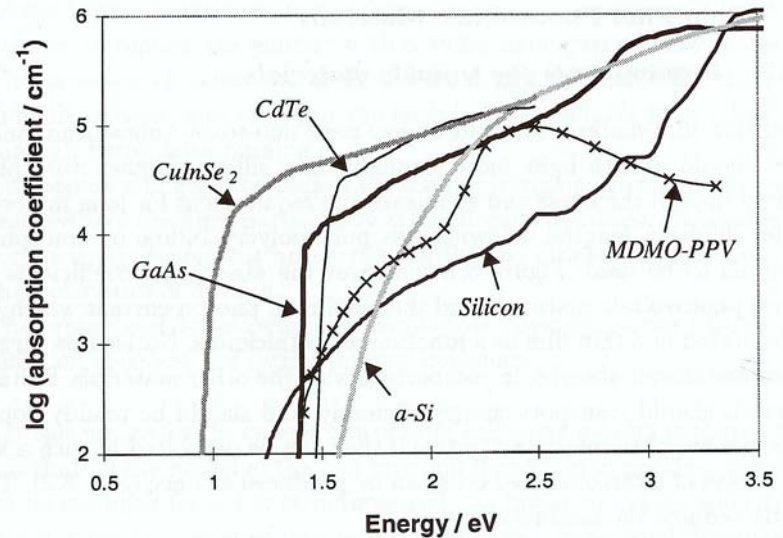
- easily controlled p and n doping (remember that Fermi energies close to the valence and the conduction bands are needed), allowing the p-n junction to be formed with the Si crystal.
- manufacturing processes available from the microelectronics industry.

Thin-film solar cells

use direct-gap semiconductors to reduce thickness of semiconductor (target: well below $1\text{ }\mu\text{m}$).

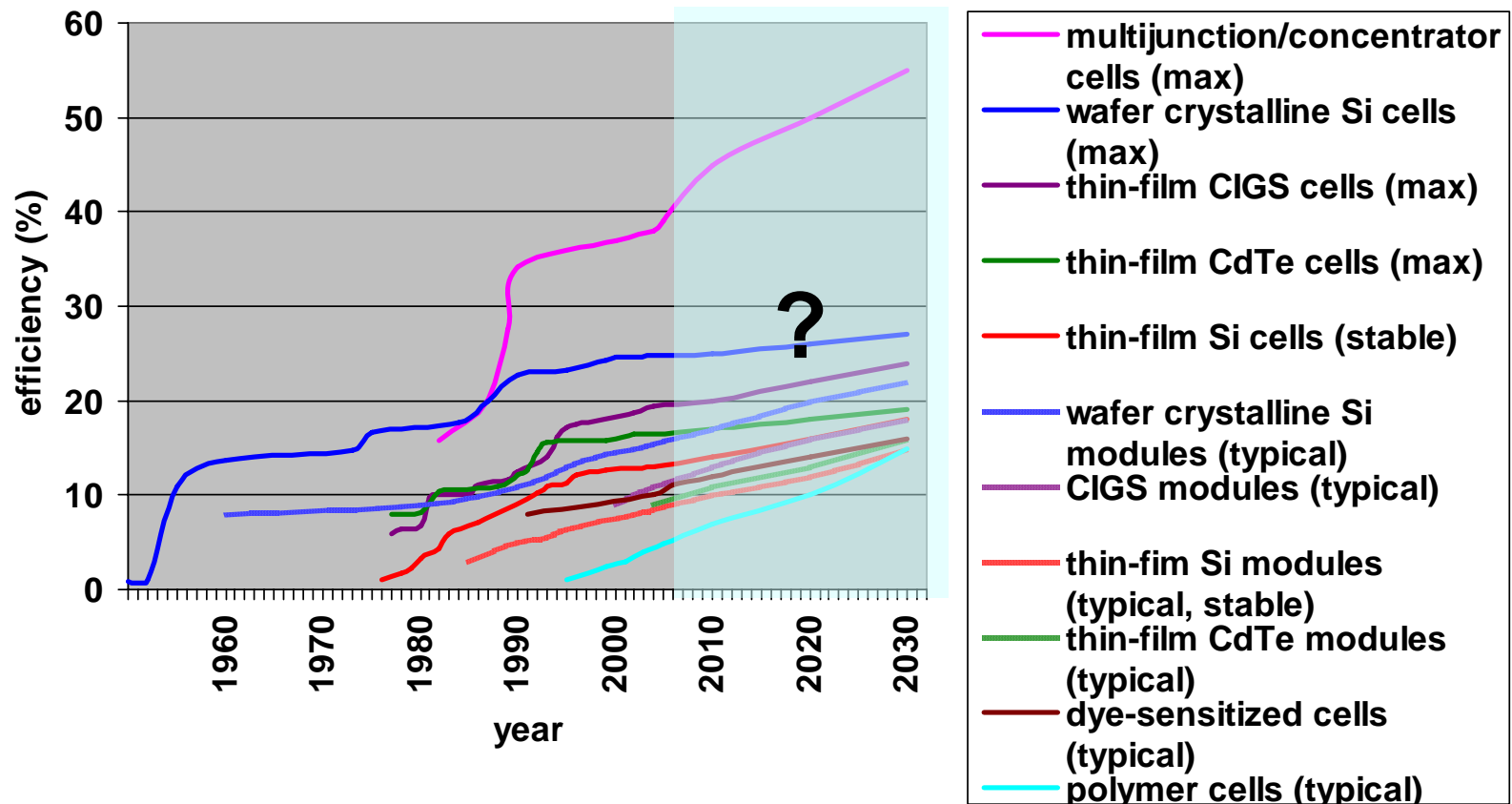
Materials investigated:

- amorphous silicon. Non-crystalline structure causes strongly-allowed absorption at the band gap (around 1.5 eV)
- III-V semiconductors. GaAs has bandgap of 1.43 eV which can be adjusted by alloying with e.g. AlAs
- CdTe
- CuInSe_2 (and alloys with Ga, CIGS)



Jenny Nelson, Physics of Solar Cells

Photovoltaic Cells: Different technologies & efficiencies (as presented at the Carbon Trust, Feb. 2007)



Amorphous silicon

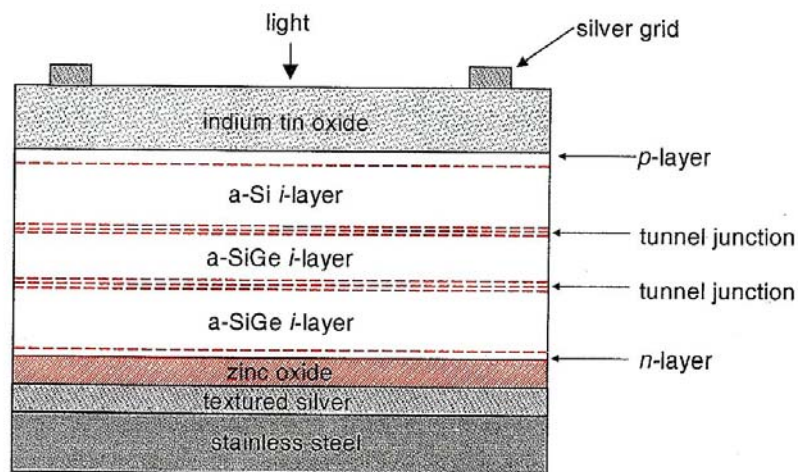
- Deposition of thin films by RF plasma decomposition of silane (SiH_4) allows manufacture of thin films which still contain large amounts of hydrogen – essential to avoid high concentrations of defect states with energy levels in the band gap (Si ‘dangling’ bonds at mid-gap), but a source of instability. Doping both p- and n-type is possible (e.g. by incorporation of phosphine, PH_3 , during growth, but is limited [Spear and Le Comber, Dundee].
- Manufacturing process technology now developed for thin-film transistors, used for active-matrix LCD display backplanes. [However, TFTs use very thin Si films and do not require multiple doping steps.] Thin-film processing still needs moderate temperatures ($>200^\circ\text{C}$) so manufacture onto glass is common, but interest also in manufacture onto ‘flexible’ steel sheets.
- Disorder causes electrons and hole energy states to be spatially localised, so that electronic mobilities are much lower than in crystalline Si [Field-effect mobilities are 100 to 1000 times lower], and associated diffusion ranges are much lower [typically $0.1\ \mu\text{m}$].

Amorphous silicon

a-Si cells are usually p-i-n, with charge photogeneration in the 'insulator' region (very light doping), and ineffective generation in the doped regions. Charge collection requires the presence of an electric field in the 'i' region (drift, rather than diffusion). 'i' regions are no more than 1 nm thick, and 'stacked' devices are now favoured in order to get better light absorption.

Open circuit voltages are low – partly because n and p doping does not bring the Fermi energy close to the band edges, and partly because E field is dropped across the 'i' regions.

Solar conversion efficiencies – up to about 12%, but not long-term stable.



'stacked' a-Si cell – 3 diodes stacked vertically. Note that the band-gaps have been tuned, with larger gap at front, and lower gap (some Si replaced with Ge) for diodes at the back

CdTe and CIGS

National Renewable Energy Laboratory, Boulder, Colorado:
Noufi and Zweibel – review of CdTe and CIGS:

Cell fabrication by successive deposition of layers of semiconductors and electrodes.

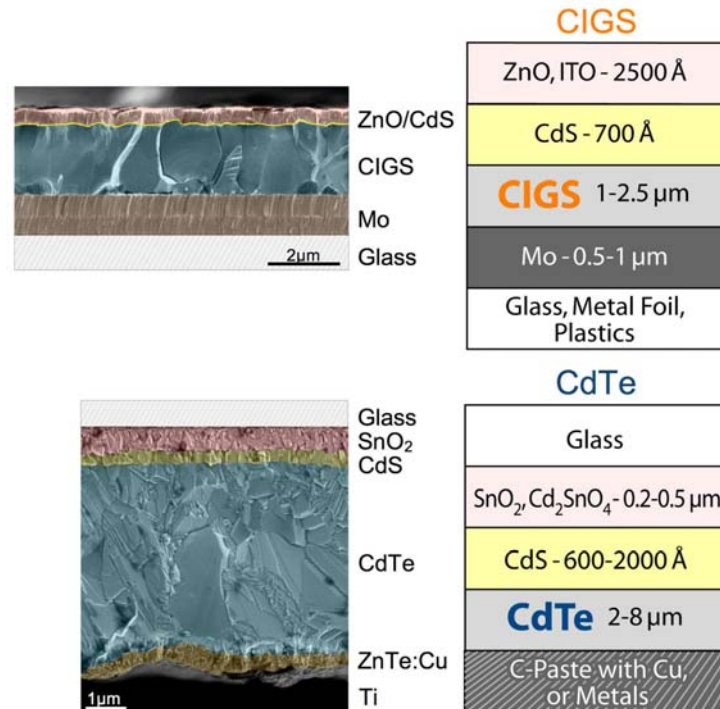
Varying band-gaps are used to arrange transparent top electrode (indium-tin or tin oxide) and 'emitter' layers: CdS on CIGS and on CdTe.

p- and n-doping is often achieved by materials selection – CIGS and CdTe are grown p-type, and CdS n-type. However, microcrystalline materials have many crystalline boundaries which reduce carrier mobility and introduce defect sites which allow recombination. Defects are particularly important at the heterojunction between different materials (lattice constants generally do not match, so grain boundaries are unavoidable)

Individual cell efficiencies are high:

CIGS to 20%

CdTe to 16.5%



CdS as 'window' layer. Absorption edge at 2.45 eV, so does block green/blue, and must be kept thin. Grows n-type without intervention

Substantial investment in thin-film solar – e.g. Nanosolar

Press release: Dec. 2006

“Makers of a new kind of solar power cell have chosen San Jose as the site of their first large-scale factory in America.

Nanosolar Inc. will occupy a former Cisco Systems facility in south San Jose, converting it into a manufacturing plant for "thin-film" solar cells, which are produced in narrow flexible sheets. The company, based in Palo Alto, also will open a factory in Germany, the world's largest market for solar technology.

The \$102 million plant on San Jose's Hellyer Avenue will make enough solar cells each year to generate 400 megawatts of electricity, roughly enough to light 300,000 homes. The facility will be ready for commercial production next year.

Unlike the standard solar cell, Nanosolar's don't use silicon. Instead, a blend of metals including copper and gallium is placed on metal foil in a process much like printing. The solar film is 100 times thinner than a silicon wafer but can produce roughly the same amount of energy.”

Market leader (2007) is First Solar CdTe manufacture on glass substrates